



# UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE  
United States Patent and Trademark Office  
Address: COMMISSIONER FOR PATENTS  
P.O. Box 1450  
Alexandria, Virginia 22313-1450  
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/488,752	01/21/2000	S. Paul Tucker	10991620.1	4859

7590 04/22/2004

Hewlett-Packard Company  
Intellectual Property Administration  
P O Box 272400  
Fort Collins, CO 80528-9599

EXAMINER

NGUYEN, PHU K

ART UNIT	PAPER NUMBER
----------	--------------

2671

DATE MAILED: 04/22/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

# Office Action Summary

Application No.

09/488,752

Applicant(s)

TUCKER ET AL.

Examiner

Phu K. Nguyen

Art Unit

2671

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

## Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

## Status

- 1) ☒ Responsive to communication(s) filed on 22 January 2004.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

## Disposition of Claims

- 4) ☒ Claim(s) 1-10 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-10 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

## Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

## Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
  - ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

## Attachment(s)

- 1) ☐ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  
Paper No(s)/Mail Date \_\_\_\_\_.

- 4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date. \_\_\_\_\_.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: \_\_\_\_\_.

Art Unit: 2671

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 1-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lawless et al. (5,371,514) in view of Kim et al. (5,355,443).

As per claim 1, Lawless teaches the claimed "display system" comprising:

"a memory, containing graphics data, divided into logical regions" (Lawless, column 5, lines 22-48); and

"an attribute system, connected to said memory wherein said attribute system automatically selects graphics data from fewer than all of said logical regions and transmits said graphics data to a display" (Lawless, column 6, lines 3-31).

It is noted that Lawless does not explicitly teach the "frame buffer attribute data" as claimed. However, Kim teaches that such frame attribute for the arrangement of stored data in the buffer is well known (Kim, column 18, lines 24-46). Thus, it would have been obvious to a person of ordinary skill in the art at the time the invention was made, in view of the teaching of Kim, to configure Lawless' system as claimed by the arrangement of different portions of the frame data in Lawless (e.g., figure 8) to define "frame buffer attribute" for the arrangement of stored data in the buffer as claimed because such arrangement improves the efficiency of the use of memory.

Applicant's arguments filed January 22, 2004 have been fully considered but they are not deemed to be persuasive. Applicant argues that Kim does not teach the claimed Applicant's invention where for any given window size and location, "there are multiple logical regions of frame buffer memory to select between for display". However, such feature is neither showed nor inherent in the claim; whereas the claim includes only "frame buffer attribute data for each pixel of a monitor" which Kim teaches in column 18, lines 28-29. Applicant argues, "an attribute system that automatically selects graphics data from fewer than all of said logical regions based on said attribute data are distinguished from the cited references" which is not correct. Kim's display region of which frame buffer data will be displayed on the video monitor (figure 4, VRAM 12) shows the frame buffer attribute data which allows the selection of graphics data from fewer than all of said logical regions of memory 56. It is clear that the displayed data on the video buffer VRAM 12 will be "fewer" than the data in the logical regions of memory 56.

Claim 2 adds into claim 1 the store of graphics data and frame attribute data in separate physical memories which Kim teaches in figure 8 and Lawless suggests in figures 3 and 8. Applicant argues that "neither Lawless nor Kim discloses attribute data capable of distinguishing between logical regions of frame buffer memory on a per-pixel basis" which is not correct because Kim's frame buffer 12 contains the attribute data capable of distinguishing between logical regions (figure 4, the attribute data in the

frame buffer 12 capable of distinguishing between logical regions of memories 50 and 56).

As per claim 3 Lawless teaches the claimed "display system" comprising:

"a memory, containing graphics data, divided into logical regions" (Lawless, column 5, lines 22-48); and

"a regions system, that calculates which regions of said graphics data contain data necessary for display of a block of pixels; wherein said regions are fewer than all of said logical regions" (Lawless, column 6, lines 3-31).

It is noted that Lawless does not explicitly teach the "frame buffer attribute data" as claimed. However, Kim teaches that such frame attribute for the arrangement of stored data in the buffer is well known (Kim, column 18, lines 24-46). Thus, it would have been obvious to a person of ordinary skill in the art at the time the invention was made, in view of the teaching of Kim, to configure Lawless' system as claimed because the arrangement of different portions of the frame data in Lawless (e.g., figure 8) can be used to defines "frame buffer attribute" for the arrangement of stored data in the buffer as claimed. Applicant argues that Kim does not teach the claimed Applicant's invention where for any given window size and location, "there are multiple logical regions of frame buffer memory to select between for display". However, such feature is neither showed nor inherent in the claim; whereas the claim includes only "frame buffer attribute data for each pixel of a monitor" which Kim teaches in column 18, lines 28-29.

Applicant argues, "an attribute system that automatically selects graphics data from

Art Unit: 2671

fewer than all of said logical regions based on said attribute data are distinguished from the cited references" which is not correct. Kim's display region of which frame buffer data will be displayed on the video monitor (figure 4, VRAM 12) shows the frame buffer attribute data which allows the selection of graphics data from fewer than all of said logical regions of memory 56. It is clear that the displayed data on the video buffer VRAM 12 will be "fewer" than the data in the logical regions of memory 56.

Claim 4 adds into claim 3 the store of graphics data and frame attribute data in physically separate memories which Kim teaches in figure 8 and Lawless suggests in figures 3 and 8.

Claim 5 adds into claim 3 "wherein said regions system sends identities of said regions to a screen refresh unit; and wherein said screen refresh unit, calculates memory addresses from said identities and sends selected graphics data from said memory to a display" which Lawless teaches in column 11, lines 34-49.

Claim 6 adds into claim 5 "said logical regions further comprising memory to store graphics data for each pixel of a monitor" which Kim teaches in figure 8 and Lawless suggests in figures 3 and 8.

As per claim 7, Lawless teaches the claimed "method for selectively reading pixel data from a frame buffer memory array" comprising:

"defining a plurality of regions of frame buffer memory, wherein each region comprises memory to store graphics data for each pixel of a monitor" (Lawless, column 5, lines 22-48); and

"calculating a subset of said regions of frame buffer memory that are required to display said pixel on said monitor; and retrieving from said frame buffer memory pixel data only from said subset of regions of frame buffer memory that are required to display said pixel on said monitor" (Lawless, column 6, lines 3-31).

It is noted that Lawless does not explicitly teach the "storing attribute data for each pixel in a memory, wherein said attribute data encodes which of said regions are to be displayed on said monitor; retrieving said attribute data for a pixel from said memory" as claimed. However, Kim teaches that such pixel attribute for the arrangement of stored data in the buffer is well known (Kim, column 18, lines 24-46). Thus, it would have been obvious to a person of ordinary skill in the art at the time the invention was made, in view of the teaching of Kim, to configure Lawless' system as claimed because the arrangement of different portions of the frame data in Lawless (e.g., figure 8) can be used to defines "attribute data encodes which of said regions are to be displayed on said monitor" for the arrangement of stored data in the buffer as claimed. Applicant argues that Kim does not teach the claimed Applicant's invention where for any given window size and location, "there are multiple logical regions of frame buffer memory to select between for display". However, such feature is neither

showed nor inherent in the claim; whereas the claim includes only "frame buffer attribute data for each pixel of a monitor" which Kim teaches in column 18, lines 28-29.

Applicant argues, "an attribute system that automatically selects graphics data from fewer than all of said logical regions based on said attribute data are distinguished from the cited references" which is not correct. Kim's display region of which frame buffer data will be displayed on the video monitor (figure 4, VRAM 12) shows the frame buffer attribute data which allows the selection of graphics data from fewer than all of said logical regions of memory 56. It is clear that the displayed data on the video buffer VRAM 12 will be "fewer" than the data in the logical regions of memory 56.

Claim 8 adds into claim 7 "wherein said graphics data and said attribute data are stored in said frame buffer memory" which Kim teaches in figure 8 and Lawless suggests in figures 3 and 8.

As per claim 9, Lawless teaches the claimed "method for selectively reading pixel data from a frame buffer memory array" comprising:

"defining a plurality of regions of frame buffer memory, each region further comprising memory to store graphics data for each pixel of a monitor" (Lawless, column 5, lines 22-48); and

“calculating a subset of said regions of frame buffer memory that are required to display said tile on said monitor; and retrieving from said frame buffer memory pixel data only from said subset of regions of frame buffer memory that are required to display said tile on said monitor” (Lawless, column 6, lines 3-31).

It is noted that Lawless does not explicitly teach the “storing attribute data for each pixel in a memory, encoding which of said regions are to be displayed on said monitor using the attribute data; defining groups of pixels as tiles; selecting a tile for display on said monitor; retrieving said attribute data for said tile from said memory” as claimed. However, Kim teaches that such pixel attribute for the arrangement of stored data in the buffer is well known (Kim, column 18, lines 24-46). Thus, it would have been obvious to a person of ordinary skill in the art at the time the invention was made, in view of the teaching of Kim, to configure Lawless’ system as claimed because the arrangement of different portions of the frame data in Lawless (e.g., figure 8) can be used to defines “attribute data encodes which of said regions are to be displayed on said monitor” for the arrangement of stored data in the buffer as claimed. Applicant argues that Kim does not teach the claimed Applicant’s invention where for any given window size and location, “there are multiple logical regions of frame buffer memory to select between for display”. However, such feature is neither showed nor inherent in the claim; whereas the claim includes only “frame buffer attribute data for each pixel of a monitor” which Kim teaches in column 18, lines 28-29. Applicant argues, “an attribute system that automatically selects graphics data from fewer than all of said logical regions based on said attribute data are distinguished from the cited references” which

Art Unit: 2671

is not correct. Kim's display region of which frame buffer data will be displayed on the video monitor (figure 4, VRAM 12) shows the frame buffer attribute data which allows the selection of graphics data from fewer than all of said logical regions of memory 56. It is clear that the displayed data on the video buffer VRAM 12 will be "fewer" than the data in the logical regions of memory 56.

Claim 10 adds into claim 9 "wherein said graphics data and said attribute data are stored in said frame buffer memory" which Kim teaches in figure 8 and Lawless suggests in figures 3 and 8.

This action has been made NON-FINAL.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Phu K. Nguyen whose telephone number is (703)305 - 9796. The examiner can normally be reached on M-F 8:00-4:30.

The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Art Unit: 2671

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Phu Nguyen  
April 16, 2004

*Phu Nguyen*  
PHU NGUYEN  
ATTORNEY  
04/16/04